# 2018-2019 Annual Report NSF NeTs Small RUI Grant

Federal Agency and Organization Element to Which Report is Submitted: 4900 Federal Grant or Other Identifying Number Assigned by Agency: 1816197

#### **Project Title:**

NeTS: Small: RUI: Bulldog Mote- Low Power Sensor Node and design Methodologies for Wireless Sensor Networks

#### **PD/PI Name:**

Nan Wang, Principal Investigator Woonki Na, Co-Principal Investigator

#### **Recipient Organization:**

California State University-Fresno Foundation

#### **Project/Grant Period:**

10/01/2018 - 09/30/2021

#### **Reporting Period:**

10/01/2018 - 09/30/2019

Submitting Official (if other than PD/PI): N/A Submission Date: 08/31/2019

Resubmit: 10/01/2019

Signature of Submitting Official (signature shall by submitted in accordance with agency specific instructions):

Naur

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## 1. Accomplishments

Project website has been built and linked under our college website.

From college website: <u>http://fresnostate.edu/engineering/research/index.html</u> (Click one of the two banners) Direct Link: http://fresnostate.edu/engineering/research/bulldogmote/index.html

Direct Elink. <u>http://itesitesitete.edu/engiteeting/reseuren/outdogitote/</u>

#### 1.1 What are the major goals of the project?

The major goals of the project are the design and implementation of the following components: (1) efficient low-power methodologies implemented throughout all WSN design layers from application to the physical layer, (2) a new WSN sensor node, the Bulldog Mote, created using various low power methodologies, and (3) energy harvesting technologies for sensor node architecture.

# **1.2** What was accomplished under these goals (you must provide information for at least one of the four categories below)?

1.2.1 Major Activities

1.2.1.1 The Wireless Sensor Network communication protocols were simulated in software to observe how the individual motes interact under varying configurations.

- a) Simulation of WSN communication protocols design and simulation, leading to publications of two IEEE conference papers.
- b) Sensor sampling and processing design.

#### • Background

Various sensors are tested and sampled through the sampling and holding circuit. Signals are then amplified to display on an oscilloscope. The goal is to study the characteristics of analog signals and methods of amplification.

• Measurement Experiments

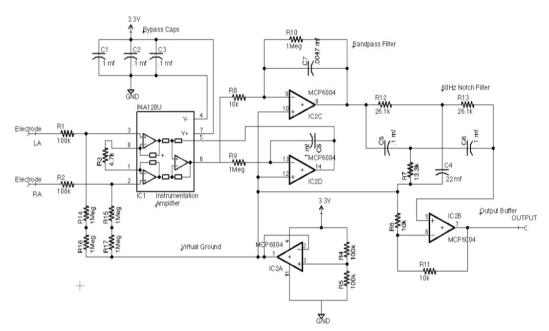
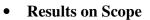


Fig.1. The Proposed Circuit Schematic

• Amplifier Circuit



#### Fig.2. Amplifier Circuit



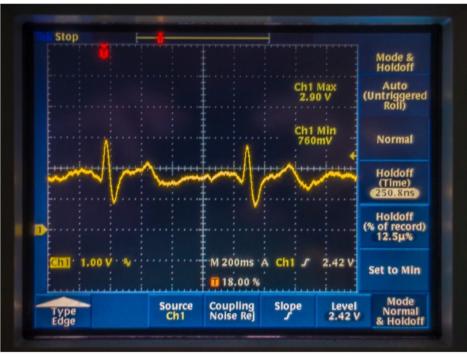


Fig.3. An analog signal

- c) Wireless sensor communication and connection experiments.
- d) WSN gateway and protocol design on physical network.
- \* Detailed information can be found in the attached file.

1.2.1.2 Energy harvesting systems were designed with careful consideration regarding the amount of energy harvested from solar power.

- a) Energy harvesting circuit design and simulation, leading to publications of two IEEE conference papers.
- b) Power management and control designs.

#### Background

Energy harvesting systems must be designed meticulously, as the amount of energy harvested can often be miniscule and/or irregular. If the system is to operate continuously, it must consume less energy than what's immediately available in its surroundings. It must also have means of storing excess energy that isn't used immediately and means for regulating the power delivered to the load. Multiple energy resources could be possible for the project, however for the first year of the project, solar power was chosen as the energy source as it provides the best available power density at an average value of 1000W/m<sup>2</sup>. Though the theoretical maximum efficiency of a solar cell is approximately 33.7%, its affordability and practicality makes it one of the most popular choices for renewable energy harvesting.

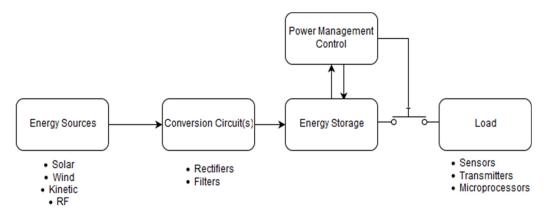


Fig. 4 General block diagram of an energy harvesting system

As seen in in Fig. 4, the efficiency of the panel can be boosted by impedance matching its load in order to maximize the power delivered. This method of control is under the class of algorithms known as maximum power point tracking (MPPT). As the name implies, the tracking algorithms continuously monitor power delivered by the panel to a load and dynamically changes the panels operating voltage to maximize this value, assuming it doesn't exceed load limitations.

Two of the most popular MPPT algorithms are Perturb & Observe (P&O) and Incremental Conductance (IC), both of which offer good performance considering their relatively simple design. The algorithms can be implemented via hardware but are normally implemented digitally using microcontrollers as they require precise numerical analysis of voltage and current levels in the system. The power conversion circuit will be a DC/DC two-switch buck/boost converter, which regulates the charge voltage and current supplied to the battery, implementing a constant current/constant voltagecharging scheme (CC/CV). Once fully charged, the battery will provide power to the mote. This requires a feedback control system, which must be able to regulate both current and voltage at or below  $a \pm 1\%$  error.

#### • Power management design

A two switch buck-boost converter in Fig. 5 was chosen for its ability to handle a wide range of input voltages while maintaining a constant output. It was also chosen for its relatively simple design requiring fewer components than the Cuk or Zeta converter topologies. Buck-boost operation is necessary as the voltage from the panel is non-linear in relation to the power drawn from it, and can vary drastically depending on environmental and load conditions. The converter will switch between buck mode (duty applied to Q1, Q2 is open) or boost mode (Q1 is always closed, duty is applied to Q2), but never buck-boost mode where both switches are being actively driven, which minimizes switching losses in the circuit and the stress on the MOSFETs, while also greatly simplifying the converter's controller design.

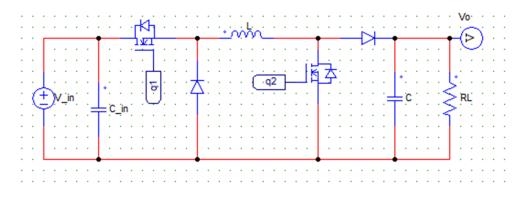


Fig.5 Two-Switch Buck-Boost Converter

The power stage was designed to keep a tight regulation on the voltage and current ripple in order to maximize the battery safety and efficiency. To minimize the size of components and reduce the voltage and current ripple on the output, a switching frequency of 100 kHz was chosen. The maximum duty cycle D<sub>Max</sub> was derived from analyzing the converter under its most strenuous conditions.  $D_1$  and  $D_2$  are the duty cycle ratios applied to switches Q1 and Q2 respectively. From this, we determined the maximum duty cycle in boost mode to be about 20% with an input voltage of 3.0V and an output of 4.2V. The maximum output current, I<sub>O, Max</sub> occurs at this duty value, which gives an average inductor current value of about 750 mA. The system was planned to store its energy using 1100 mAh polymer Li-Ion battery, which would provide power for the sensor mote when more is needed from the solar panel. A polymer Li-Ion battery was chosen for its high energy density. In order to maximize the batteries capacity and longevity, a two- stage constant current/constant voltage charging process was required, as seen in Fig. 6. In this method, the battery is charged at a constant current, typically 0.5C A (half the maximum capacity) until it reaches its maximum voltage, typically 4.2 V. Once it reaches the maximum voltage, the charger should switch into constant voltage

mode. Both phases require the applied current or voltage to be within 1% error. The battery will complete charging once the battery current goes down to 0.1C and the battery voltage is at maximum. Both current and voltage control can be accomplished by adjusting the reference voltages of the converter's voltage feedback controller accordingly using samples taken from voltage or current sensors. When there is sufficient power being provided from the solar panel, the system will redirect that power to the sensor module to perform its operations. This way, the system will minimize its use of the battery and extend battery life.

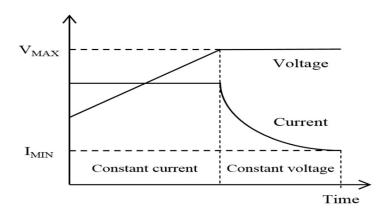


Fig. 6 CC/CV charging scheme

(researchgate.net/figure/Constant-current-constant-voltage-charging-profile-for-a-single-battery-cell\_fig6\_290358853)

It is also necessary to monitor the amount of charge that has been applied to the battery and its estimated state of charge (SOC) in order to avoid damage to the lithium ion battery. It is generally best not to fully charge a lithium battery to avoid the risk of damaging it. The simplest way of determining the state of charge is through the use of coulomb counting. Coulomb counting integrates battery current in order to determine the state of charge as seen in equation 1, where Ib is the battery current, I<sub>Loss</sub> is the current consumed by loss reactions, C<sup>r</sup>rated is the capacity of the battery in Ah, and SOC (*to*) is the initial state of charge.

$$SOC = SOC(t_0) + \frac{1}{C_{\text{rated}}} \int_{t_0}^{t_0 + \tau} (I_b - I_{\text{loss}}) dt$$
(1)

The initial state of charge must be determined beforehand in order to have an accurate starting point for the charging algorithm. If enough time has elapsed (approximately 4 hours), the SOC of the battery could be determined by using the open circuit voltage of the battery, which is directly proportional to its state of charge. If all battery properties are provided, PSIM is capable of providing the proportional relationship between the two as seen in Fig.7. As the constant current used to charge the battery decreases, the battery takes longer to reach maximum voltage, saturation, and subsequently constant voltage mode.

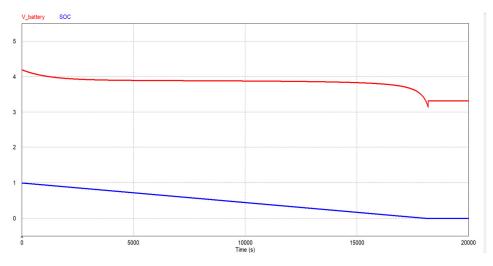


Fig.7 The SOC of the battery & terminal voltage vs time in seconds (discharging)

Fig. 8 shows the proposed flowchart of the intended charging scheme of the battery within the microcontroller. The microcontroller could implement the closed loop control for the DC/DC converter using its internal op-amps to implement an error amplifier and a type-III compensation controller.

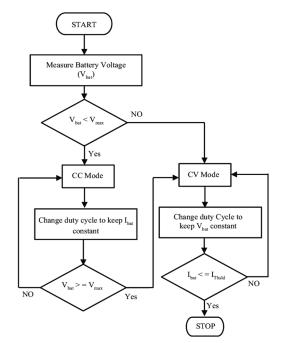


Fig.8 The flow chart of the charging control algorithm.

#### • Control design

Fig. 9 is the proposed controller design for the two-switch buck-boost converter. The simplified C block (SSCB) was used to implement the functions of the microcontroller for the PSIM simulations. The output voltage of the converter is compared to a reference generated by the control block 'Regulator'. The error voltage then passes through the type-III compensator and through the limiter. The control signal from the limiter then

goes into a comparator which generates the PWM control signal using a 100 kHz 1.8V amplitude saw-tooth carrier wave. The converter mode is determined by comparing the output and input voltages, which determines which switch is actively controlled. The design will utilize a single voltage control loop in order to minimize the complexity of the circuit. It is necessary to design the controller so that the system is stable at its the extreme operating conditions. Fig. 12 shows the power-stage bode plot under varying load and input voltage conditions. The phase margin for the controller was set in the range of 45° to 50° with a cutoff frequency of 1.8kHz. The power stage transfer function is given in equation (2), which considers the DC resistance of the inductor  $R_L$  and the ESR of the capacitor rc. Ro is the output load resistance of the converter,  $V_{O,max}$  is the max DC output voltage (4.2V),  $I_{in}$  is the corresponding DC input current and D is the corresponding duty cycle.

$$G_{PS}(s) = \frac{v_o(s)}{d(s)} = \frac{V_{O,max} - (Z_L \cdot I_{in})/(1-D)}{(1-D) + Z_L/[Z_O \cdot (1-D)]}, Z_L = sL + R_L, Z_O = \frac{R_O(1+sCr_C)}{1+s(R_L + r_C)C}$$
(2)

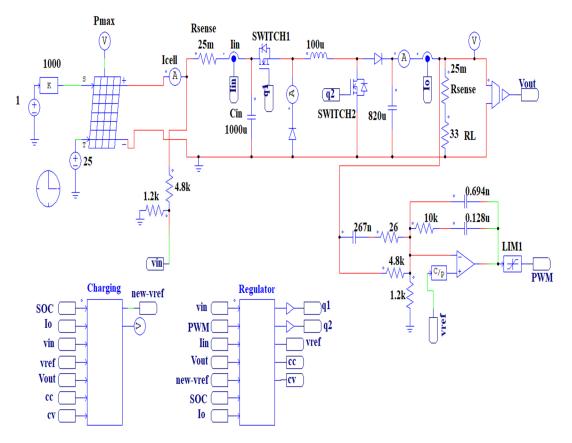


Fig.9 Proposed system design, designed in PSIM

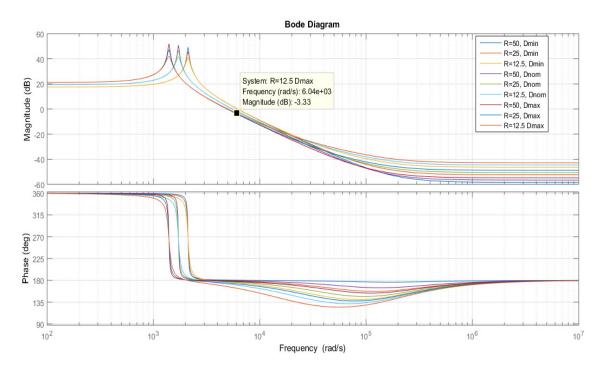


Fig. 10 Power stage transfer function based on varying operating conditions.

The power stage requires a rather large phase boost past 1000 rad/s so a type-III compensator was chosen in order to provide a 150° phase boost. The compensator is implemented using an RC network and an op-amp acting as a differential amplifier in Fig. 10.

#### 1.2.2 Specific Objectives

a. This could be a simple 3-node wireless senor network that measures ambient temperature, light, and humidity. The idea is to get this infrastructure working on a small scale and then scale up. The sensor nodes can be connected via various methodologies, but the most basic one is called the Star Method. It consists of a sensor mote connected out to each of the individual nodes. The sensor mote is also known as a gateway or base unit. This is the crux of the connection between the physical sensor nodes and the cloud connection. Each node can talk back and forth with the sensor mote, but they cannot laterally talk to each other. That feature is definitely sought after for certain applications, but for right now ours does not require that functionality.

b. The power conversion circuit for the energy harvesting will be a DC/DC two-switch buck/boost converter, which will regulate the charge voltage and current supplied to the battery, implementing a constant current/constant voltage charging scheme (CC/CV). Once fully charged, the battery will provide power to the mote. This requires a feedback control system, which must be able to regulate both current and voltage at or below a  $\pm 1\%$  error.

#### 1.2.3 Significant Results

a. The wireless sensor mote for this project has been verified to be capable of sensing accurate changes to temperature and light intensity as well as being able to communicate with other motes for the development of the wireless sensor network. The wireless sensor network itself has not been established however, but the sensors were found to be able to obtain data in real time, as well as broadcast to all other motes within a 300 foot range given no obstacles.

b. A successful simulation of the controller for energy harvesting using solar energy was implemented to produce constant current and constant voltage. A successful prototype for the two-switch buck-boost converter for the energy harvesting has also been created, but still requires the implementation of the closed loop control. Also in order to minimize the noise, PCB design would be required.

- 1.2.4 Key outcomes or other achievements
  - 1. 3-node wirelsess node network design and simulation

## \* Detailed information can be found in the attached file.

2. An energy harvesting circuits and its control algorithm

# 1.3 What opportunities for training and professional development has the project provided?

- The PI, Dr. Nan Wang participated in the IEEE ICCC 2018 conference in Chengdu, China, December 2018 and IEEE ICCSN 2019 conference in Chongqing, China, June 2019 to deliver keynote speaking on the NSF NeTs Bulldog project and present the papers.
- Harshdeep Jhajj, graduate student, attended the IEEE CCWC 2019 conference in Las Vegas, USA to present one paper.
- The co-PI, Dr. Woonki Na participated in the IEEE ICPE 2019 conference in Busan, Korea, May 2019 to present the paper.
- The co-PI, Dr. Woonki Na participated in the IEEE APEC 2019 conference in Anaheim, USA, Mar. 2019 to present the paper.

## 1.4 How have the results been disseminated to communities of interest?

- The PI, Dr. Nan Wang delivered keynote speaking on the NSF NeTs Bulldog project and presented the related papers in the IEEE ICCC 2018 and IEEE ICCSN 2019 conferences held in China.
- The co-PI, Dr. Woonki Na participated in the IEEE ICPE 2019 conference in Busan, Korea, May 2019 to present the paper.
- The co-PI, Dr. Woonki Na participated in the IEEE APEC 2019 conference in Anaheim, USA, Mar. 2019 to present the paper.

- Harshdeep jhajj, graduate student, attended the 40th Central California Research Symposium, Fresno, California, April, 2019, to present his work.
- A project webpage has been created on the college website, accessible from anywhere in the world.
- This project idea is disseminated during Project day held in Fresno, CA on May 7
- **Project website has been built and linked under our college website.** From college website: <u>http://fresnostate.edu/engineering/research/index.html</u> (Click one of the two banners) Direct Link: http://fresnostate.edu/engineering/research/bulldogmote/index.html

## 1.5 What do you plan to do during the next reporting period to accomplish the goals?

- New WSN communication protocols will be studied and simulated.
- WSN will be formed by sensor nodes; and low power communication protocols will be tested to gather results.
- Analog signal sampling and processing will be implemented.
- Complete control design will be studied and implemented.
- Using other power sources such as wind, vibration and a combination of other energy storage will be studied and implemented.
- A PCB design for the power management will be tested and completed.

# 2. Products

## 2.1 Conference papers

- 1. N. Wang, R. Datla and H. Jhajj, "NCMDSDV: A Neighbor Coverage Multipsth DSDV Routing Protocol Design for MANETs", in Proc. The 11th IEEE International Conference on Communication Software and Networks (ICCSN 2019), Chongqing, China, 06/2019.
- 2. H. Jhajj, R. Dalta, and N. Wang, "Design and Implementation of An Efficient Multipath AODV Routing Algorithm for MANETs", in Proc. the 9th IEEE Annual Computing and Communication Workshop and Conference (IEEE CCWC 2019), Las Vegas, NV, USA, January 2019, pp. 895-899.
- 3. S. K. Pasumarthi, G. Fei, and N. Wang, "EHTC: An Enhanced Huffman Tree Coding Algorithm and its FPGA Implementation", accepted to the 4th IEEE International Conference on Computer and Communications (IEEE ICCC 2018), Chengdu, China, December, 2018.
- 4. A. Basavarji, W. Na, N. Wang, J. Kim and T. Kim, "Control of Kalman Filter based Z source inverter in Photovoltaic Applications", in the Proc. IEEE ICPE 2019 conference in Busan, Korea, May 2019
- J. Park, G Kim, W. Na, C. Lim and J. Kim, "Nonlinear Observer and Simplified Equivalent Circuit Model-based EKF-SOC Estimator of a Rechargeable LiFePo4 cell," presented in the IEEE ICPE(International Conference on Power Electronics) 2019 conference in Busan, Korea, May 2019

#### 2.2 Website

**Title:** NSF NeTs Bulldog Mote Project at Fresno State. **URL:** http://fresnostate.edu/engineering/research/bulldogmote/index.html

#### Short Description of the Website

The Fresno State BullDog Project is supported by the NSF NeTs Grant #1816197, from 10/01/208 to 09/20/2021. This project aims to design a new low-power sensor node, the Bulldog Mote, using attractive low power techniques, such as energy harvesting, clock scheduling, and dynamic voltage scheduling, implemented through all WSN design layers. The impact of this project will be further strengthened by: (1) embedding low-power design technologies in substantial systems from major industry parties, (2) enhancing curriculum development with improved courses and senior projects, (3) disseminating research results through online tutorial, peer referred publications, and open-source website, (4) reaching out to K-12 students and underrepresented minority groups through open houses and summer camps, and (5) supporting women and minority students in research. Finally, subsequent comprehensive low-power design model and procedures will be developed for designers to create and improve designs of other embedded devices under tight power constrains.

## 3. Participants/organizations

## 3.1 \* What individuals have worked on the project?

- Nan Wang, Ph.D., Professor, PI
- Woonki Na, Ph.D., Associate Professor, co-PI
- Harshdeep Jhajj, Graduate Student, WSN and MANET protocol design and simulations
- Calvin Smith, Undergraduate Student, WSN Communication gateway and physical design
- Russel Skaggs-schllenberg, Undergraduate student, WSN Communication gateway and physical design
- Jared Sarajian, undergraduate student, Sensor program and communication
- Daniel Jacuinde-Alvarez, Ungraduate student, physical signal sampling and processing
- Alwin Oliver Villamor, Ungraduate student, physical signal sampling and processing
- Luis Ortega, Ungraduate student, Energy harvesting basic circuit hardware design
- Jasmin Lopez, Ungraduate student, Energy harvesting basic software design
- Cheaheng Lim, Graduate Student, Energy harvesting hardware and software design integration
- Shwetha Murali Gopika Manoharan, Graduate Student, Energy harvesting Maximum Power Point Tracking Algorithm research.

## 3.2 What other organizations have been involved as partners?

• Chungnam National University, Daejon, S. Korea

## 3.3 What other collaborators or contacts have been involved?

• Jonghoon Kim, Assistant professor, Electrical Engineering department, Chungnam National University, Daejon, S. Korea

#### 4. Impacts

#### 4.1 What is the impact on the development of the principal discipline(s) of the project?

- Enhanced ECE courses, such as senior design, embedded systems, wireless communications, networking, power systems and smart grid designs by adding up-to-date technical contents and projects.
- Improved involvement of underrepresented students in research projects.
- Enhanced learning experience of undergraduate and graduate students by involve them in real world projects.

#### 4.2 What is the impact on other disciplines?

N/A

#### 4.3 What is the impact on the development of human resources?

• Enhanced training and retention of the junior faculty.

#### 4.4 What is the impact on institutional resources that form infrastructure?

• The project will provide a method to design low power digital devices using various technologies. It can be used in teaching or device designs.

#### 4.5 What is the impact on technology transfer?

• The project will provide a method to better monitor forest fire, landslides, and structure health.

#### 4.6 What is the impact on society beyond science and technology?

- Attract students from underrepresented groups to the FSU engineering department.
- Improve students' interest in enrolling to programs at Fresno State University.