

The background of the entire page is a high-resolution, blue-tinted image of a microchip. The chip's surface is covered in a complex grid of circuitry, with various colored regions (yellow, green, red, blue) representing different functional blocks. In the lower right corner, there is a stylized white graphic of circuit traces and nodes, which appears to be overlaid on the chip image. A thick red curved line runs across the bottom of the page, separating the main content from the footer.

FRESNO
STATE

Lyles College of
Engineering

Semiconductors, ASICs, Materials

Deep Roots. Bright Futures.

Fresno State, nestled in the center of California, serves one of the most culturally diverse regions in the country. The university dates back to 1911, when the doors of the then Fresno State Normal School opened to 150 hopeful students. Today, Fresno State is serving nearly 24,000 students within its eight schools and colleges.

79% of Fresno State students are from the Central Valley, having a direct and meaningful impact on our regional economy and vitality.

Diversity, equity, inclusion and belonging are a core mission: Fresno State is a designated Hispanic-Serving Institution and an Asian American and Native American Pacific Islander Serving Institution.

66.2% of Fresno State students are the first in their families to graduate from college.

Each year, academics at Fresno State steadily garners more attention with the release of several prestigious national rankings. Reports from Washington Monthly Magazine, U.S. News and World Report and Money Magazine consistently place our University alongside some of the best universities in the US.



STUDENT DEMOGRAPHICS (fall 2022)

African American: **3%**
American Indian: **< 1%**
Asian: **12%**
Hispanic: **57%**
Pacific Islander: **< 1%**
White: **17%**
Other/unknown: **6%**
Non-resident alien: **5%**



First-generation undergraduates: **66%**



Introduction



Semiconductors, ASICs, Materials in the Lyles College of Engineering

California State University, Fresno (Fresno State) has offered engineering courses and programs since 1922. The Lyles College of Engineering currently offers seven undergraduate degree programs and five graduate degree programs including BS degree programs in Computer Engineering, Electrical Engineering and Mechanical Engineering, and MS degree programs in these areas. Minors in Electrical Engineering, Computer Engineering, and Cybersecurity are also offered.

The Lyles College has a strong history of partnerships with industry, and organizations such as the Fresno County Economic Development Corporation and the San Joaquin Valley Manufacturing Alliance, and contributes greatly to the region's economic growth. Over the past three decades, graduates of the programs have worked at companies such as Boeing Company, Intel, AMD, Apple, Tesla, Anduril, General Electric, Cisco, SpaceX, Motorola, Cruise, Amazon, IBM, Meta/Facebook, Lockheed Martin, NASA, Walt Disney Co., US Department of Energy, US Air Force, US Navy, US Army Space Command, Edwards Air Force Base, Hewlett Packard, Raytheon, Northrop Grumman, Lucent, Kawasaki, General Motors, Fujitsu, LSI Logic, Sandia National Laboratories, Honda, Texas Instruments, Qualcomm, Western Digital, Cadence, Siemens, Synopsys, Microsoft and Ford Motor Co.

The pages that follow describe the variety of courses in semiconductors, chip design and materials offered in the Lyles College of Engineering, a list of faculty and their expertise areas, and a small sample of some of the current research projects in semiconductors and advanced materials.

Detailed information about the Lyles College of Engineering's program offerings and research in semiconductors, ASICs, and materials are available at:

engineering.fresnostate.edu/semiconductors

Course Offerings in Semiconductors, Chip Design, Materials

The Departments of Electrical and Computer Engineering and Mechanical Engineering offer a variety of undergraduate and graduate courses in semiconductors, advanced materials, circuits and systems, digital and analog electronics, VLSI design, computer architecture, embedded systems, computer arithmetic, cryptography, cybersecurity, digital signal processing. Students gain valuable hands-on experience and use a variety of hardware and software tools, including advanced materials fabrication and characterization instrumentation in their learning, research and projects. Graduates are well prepared for careers in the semiconductor industry.

Undergraduate Courses

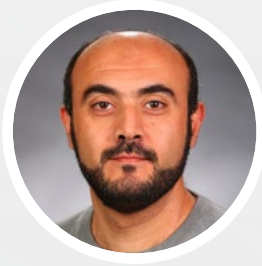
- Switching Theory and Logical Design
- Physical Electronics and Fabrication
- Analog Electronics Circuits Design and Analysis
- Analysis and Design of Digital Circuits
- VLSI System Design
- Power Electronics
- Analog Integrated Circuits and Applications
- Discrete Time Signals and Systems
- Digital Signal Processing
- Microwave Devices and Circuits Design
- Microwave Amplifier and Oscillator Design
- Quantum Electronics
- Cloud and Cybersecurity
- Advanced Digital Logic Design
- Advanced Computer Architecture
- Embedded Systems
- Fundamentals of Machine Learning
- Robotics Fundamentals
- Engineering Materials
- Fundamentals of Cryptography and Computer Network Security

Graduate Courses

- VLSI Circuits and Systems
- Digital Systems Testing and Testable Design
- VLSI Physical Design
- Advanced Hardware Design of Computer Arithmetic
- Modern Semiconductor Devices
- Embedded Systems Design
- Advanced Power Electronics
- Digital Signal Processing
- High Performance Computer Architecture
- Digital Control Systems
- Advanced Signals and Systems
- Electron Microscopy



Semiconductors Education and Research Faculty



Dr. Hayssam El-Razouk, Ph.D., University of Western Ontario

Research and Expertise: Computer arithmetic, cryptographic hardware, and digital VLSI circuits design.

Prior Experience: Engineer, RedIron Technologies, London, Ontario, Canada, research scientist with IBM Canada and Postdoc with the Electrical and Computer Engineering Department at Western University.



Dr. Soumyasanta Laha, Ph.D., Ohio University

Research and Expertise: Analog, RF and mm-wave IC Design, Wireless Network on Chip and Biomedical Circuits and Systems.

Prior Experience: Postdoctoral Researcher at Ohio University, USA, Senior Visiting Researcher at Intel Corporation, Austria, Senior Project Engineer at Indian Institute of Technology Kanpur, India and Research Associate at Newcastle University, U.K.



Dr. Zoulikha Mouffak, Ph.D., University of Houston

Research and Expertise: Semiconductor materials and device process technology.

Prior Experience: Senior Process Engineer at Intel and International Rectifier working on wide bandgap materials, especially GaN, as well as on porous silicon (P-Si) processing and characterization.



Dr. Aaron Stillmaker, Ph.D., University of California, Davis

Research and Expertise: Many-core VLSI design, digital design (Verilog), physical VLSI design, and EDA tool flows.

Prior Experience: Intel Labs in Hillsboro, OR, and California State University, Fullerton.



Dr. Nan Wang, Ph.D., University of Louisiana, Lafayette

Research and Expertise: System-on-chip/network-on-chip communication architecture, embedded systems, smart textile sensors and wireless communication.

Prior Experience: Associate Professor at West Virginia University Institute of Technology.

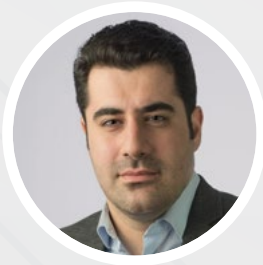
Semiconductors Education and Research Faculty



Dr. Woonki Na, Ph.D., University of Texas at Arlington

Research and Expertise: Power electronics, electric drives, and Hardware In the Loop System based control designs for hybrid electric vehicles and renewable/ alternative energy applications.

Prior Experience: Post-doctoral researcher at University of Michigan-Dearborn, Senior Engineer at Caterpillar Inc, Assistant Professor at Bradley University, IL.



Dr. Shahab Tayeb, Ph.D., University of Nevada, Las Vegas

Research and Expertise: Network security and privacy, Internet of Things (IoT), machine/deep learning techniques and data analytics approaches, zero-day attack detection. secure intra-vehicular network backbone for Connected and Autonomous Vehicles.

Prior Experience: Cisco Networking Academy



Dr. Sankha Banerjee, Ph.D., Rutgers University

Research and Expertise: Fabrication, plasma processing, and characterization of electro-active and photoactive materials for agricultural and biomedical applications.

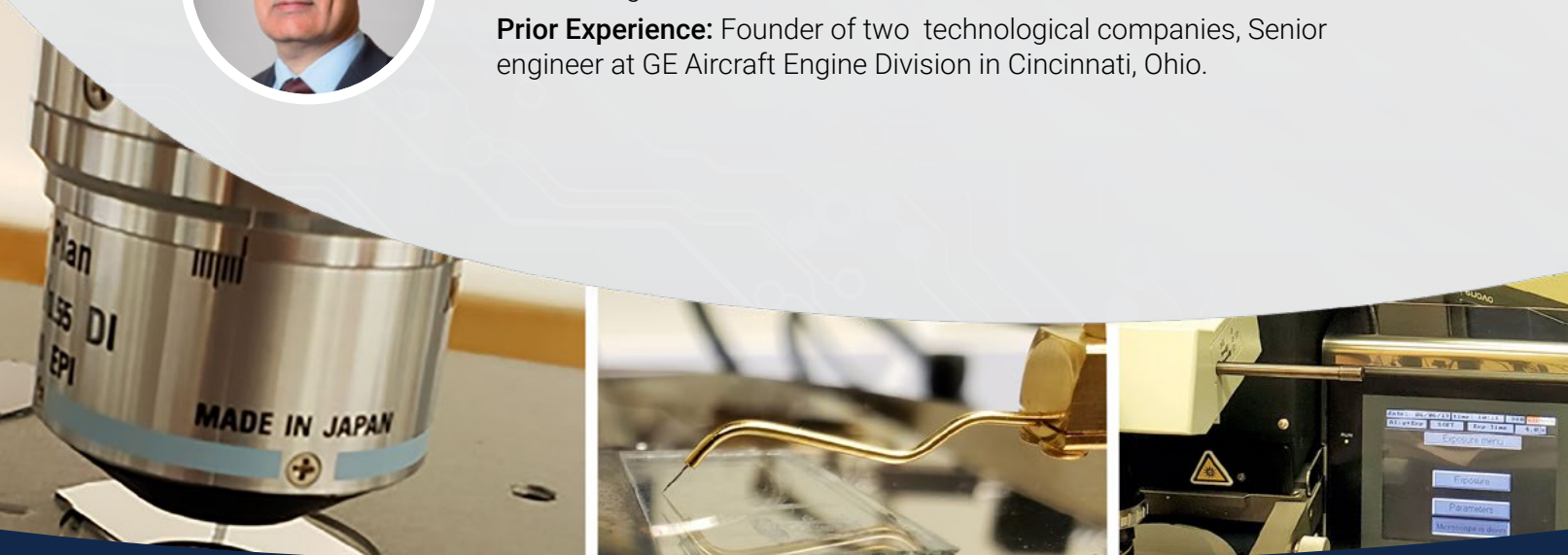
Prior Experience: Researcher at the Princeton Plasma Physics Laboratory, NJ.



Dr. Reza Raeisi, Ph.D., University of Cincinnati

Research and Expertise: Embedded Systems, VLSI Design Verification and Testing domains.

Prior Experience: Founder of two technological companies, Senior engineer at GE Aircraft Engine Division in Cincinnati, Ohio.



Runtime Reconfigurable Cognitive Spectral Processor (R2CSP)

Lead Researcher: **Dr. Aaron Stillmaker**

The project focuses on the development and fabrication of a fine-grained many-core processing runtime reconfigurable spectral processor (R2CSP) for radio frequency (RF) spectral sensing leveraging the KiloCore architecture and physical design developed by Dr. Stillmaker. Dr. Stillmaker and his team at Fresno State are responsible for the physical design of the R2CSP chip. The plan is to fabricate several test chips in TSMC's 16 nm technology. This multi-institutional project is led by Dr. David Zhang from SRI in Princeton, NJ, with Dr. Bevan Baas as a Co-PI from UC Davis. The research has received \$13 million for the two and a half-year program scheduled to end in November 2025.

Area and Energy Efficient Full Duplex Transceiver System for Wireless Network on Chip

Lead Researcher: **Dr. S. Laha**

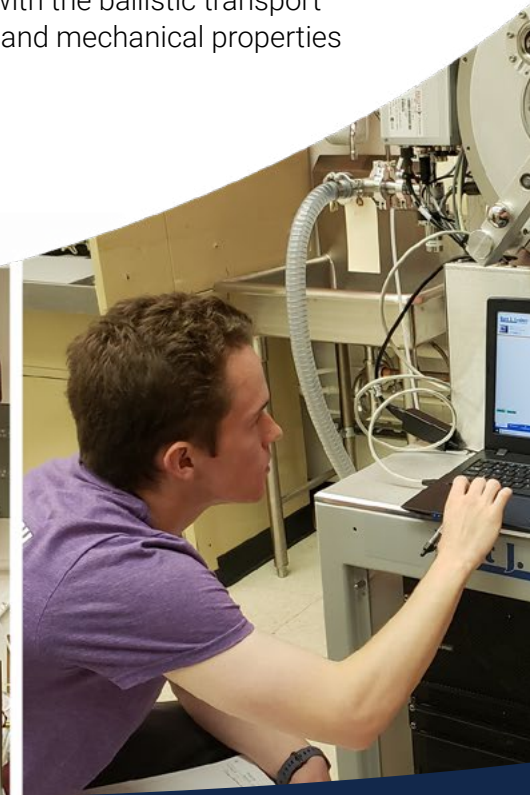
Co-time co-frequency full-duplex wireless communication alleviates the issue of inefficient use of bandwidth in the existing co-time half-duplex communication. In the full-duplex mode, the transmission and reception of the signal takes place simultaneously in the same frequency band. The primary challenge in designing such a full-duplex wireless device is self-interference. The transmit signal, which is locally generated in the transceiver and thus has a very high-power level, interferes with the low power received signal for being in the same frequency band. The received signal is thus submerged in the 'self-interfered noise' and cannot be recovered. Several techniques have been suggested over the last decade to reduce the self-interfered signal to the level where it can be neglected, thus eliminating self-interference. The current project aims to bring the self-interference cancellation to 60 dB or more, which is sufficient for on-chip wireless communication such as wireless network on chips (WiNoCs). With regards to WiNoC, this is important because, WiNoCs require high data rates (10 Gbps and beyond) to support today's high performance multi-core computer architecture and require simultaneous data transfer to support real time applications. The expected success of this research will motivate system level study with advanced sub-16 nm RF FinFET technology at 60 GHz and sub-THz frequencies to evaluate and compare the performance of existing and novel WiNoC architectures. Furthermore, the validation of the full duplex transceiver system for WiNoC applications will expand research insights for full duplex capability of other on-chip communications, such as between wireless enabled chiplets or a wireless neural accelerator architecture.

Innovative Nano-material Synthesis: toward the development, manufacturing, and characterization of cutting-edge electro-active and photoactive nanomaterials and composites, ensuring their suitability for advanced manufacturing processes

Lead Researcher: **Dr. Sankha Banerjee**

Research Project Description: This project is focused on the comprehensive creation, production, and analysis of state-of-the-art electro-active and photoactive nanomaterials and composites, ensuring their appropriateness for advanced manufacturing processes. The objectives are (i) Fabrication/Synthesis Method Optimization: Develop and optimize fabrication and synthesis methods, including simulation-based techniques, for thin films and bulk active materials such as perovskite and MXene-based material and composites. (ii) Mechanism Investigation: Explore the mechanisms influencing material properties by varying fabrication parameters and employing computational techniques. (iii) Microstructural Analysis: Investigate the effects of physical relationships between different phases in an electroactive material or composite and their impact on measured properties. (iv) Characterization and Testing: Conduct thorough characterization and testing of active nanomaterials utilizing electron microscopy and spectroscopic techniques. (v) Optimization and Tailoring: Optimize and tailor material properties and performance based on the parameters identified in the previous objectives and specific application requirements.

Sub-project Example: "Wet lab fabrication of Perovskite/Wurtzite-Oxide (e.g. ZnO, BaTiO₃) and 2D Materials-based (e.g. MXenes) flexible electro-active thin films with active polymer and co-polymer matrices (e.g. PVDF/PVDF-TrFE)" - The purpose of this project is to study the role of the dielectric and piezoelectric properties of graphene-based composite piezoelectric materials. Due to its unique electrical and mechanical properties such as it being stretchable up to 20% of its initial length and having high conductivity due to the unidirectional structure with the ballistic transport of electrons, the role of the 2D phase is critical in tailoring the electrical and mechanical properties of the multiphase composites.



Extended-Gate Field Effect Transistor (EGFET)-Based sensors

Lead Researcher: **Dr. Zoulikha Mouffak**

This research is focused on the use of a EGFET sensor as a pH sensor or specific chemical detector. We are exploring this setup to target biomedical applications. When the MOSFET is connected to a sensitive electrode through the chemical solution we want to analyze, the sensitive electrode works as an “extended gate”. Modification of the solution concentration has resulted in changes in the drain current when running I-V characteristics. We developed a *ITO/PET EGFET pH sensor* using ITO (Indium Tin Oxide)/PET (Polyethylene Terephthalate) sensing electrode as the extended gate part of an EGFET obtained from a combination of FETs from the CD4007 chip. The device was tested by immersing the ITO/PET electrode in several chemical solutions of acidic and basic nature, including hydrogen peroxide, acetic acid, sulfuric acid, and ammonium hydroxide, at different concentrations. Using a Tektronix 4200A source meter, we plotted the current–voltage (I–V) characteristics for the different chemical solutions, and we established a correlation to the pH changes. Results from the plotted I–V characteristics show a great dependence of the drain current (I_D) on solution concentration. The pH of the used solutions established a relationship between the drain current and the pH value. The results showed a consistent decrease in the current with an increase in the pH value, although with different rates depending on the solution. The device showed high voltage sensitivity at 0.23 V per pH unit when tested in sulfuric acid. These results were recently published in *Sensors*. <https://doi.org/10.3390/s23208350>

For more details on these and the following additional projects please visit:

engineering.fresnostate.edu/semiconductors



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- Prototype Shirt for Electrocardiography and Electromyography Analysis
 - Fabrication of Porous silicon (PSi) films for sensing devices
 - Porous Silicon-Based EGFET sensing electrode with interdigitated contacts
 - Bulldog Mote - Low Power Sensor Node and Design Methodologies for Wireless Sensor Networks
 - A digital twin-based condition monitoring method for power converters
 - Computer Arithmetic and Cryptographic Hardware
 - Side-Channel Leaks
 - Applied Cryptography

Recent Research Publications

1. **S. Laha, A. Rajput, S.S. Laha, R. Jadhav**, "A Concise and Systematic Review on Non-Invasive Glucose Monitoring for Potential Diabetes Management", *Biosensors (MDPI)*, vol. 12, no. 11, Nov. 2022
2. **S. Liu, T. Canan, H. Chenji, S. Laha, S. Kaya and A. Karanth**, "Exploiting Wireless Technology for Energy-Efficient Accelerators With Multiple Dataflows and Precision," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 7, pp. 2742-2755, July 2022
3. **F. Shaikh, N. Haworth, R. Wells, J. Bishop, S. Chatterjee, S. Banerjee and S. Laha**, "Compact Instrumentation for Accurate Detection and Measurement of Glucose Concentration Using Photoacoustic Spectroscopy," *IEEE Access*, vol. 10, pp. 31885-31895, 2022
4. **F. Shaikh and S. Laha**, "Frequency Characterization for Glucose Detection with Software Defined Radio," in *IEEE Wireless and Microwave Technology Conference (WAMICON)*, Melbourne, FL, USA, 2023, pp. 148-151
5. **Z. Mouffak, V. Adapala**, "Exploring the ITO/PET Extended-Gate Field-Effect Transistor (EGFET) for pH Sensing," *Sensors* 23 (20), 8350M, 2023.
6. **S. Koripalli, D. Sheela, and N. Wang**, "Optimizing Post Deployment Maintenance at Nodal Level for Macroscale Wireless Sensor Network," *2024 IEEE 14th Annual Computing and Communication Workshop and Conference (CCWC)*, Jan. 2024, Las Vegas.
7. **T. Ridley, J. Andrade, C. Luna and H. El-Razouk**, "Smart Car Temperature Monitoring System Using SRAM-Based PUF Sensor," *2024 IEEE 14th Annual Computing and Communication Workshop and Conference (CCWC)*
8. **A. Cabrera, A. Rider, J. Xiong and H. El-Razouk**, "Implementing Privacy on Public Digital Displays Using Smart Glasses," *2023 IEEE 13th Annual Computing and Communication Workshop and Conference (CCWC)*, 2023, pp. 274-279.
9. **P. Shi, A. Stillmaker and B. Baas**, "Efficient and High-Performance Sparse Matrix-Vector Multiplication on a Many-Core Array," *IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc)*, Penang, Malaysia, December 2022.
10. **R. Chen, A. Stillmaker and B. Baas**, "Architecture and 28 nm CMOS Design of a 1886 MBin/sec Context-Adaptive Binary Arithmetic Coder (CABAC) Encoder," *IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Patras, Greece, October 2022.
11. **A. Bonasu, A. Stillmaker and S. Tayeb**, "Low-Power Vehicular Network ASIC Implementation," in *Proceedings of Latin American Symposium on Circuits and Systems (LASCAS)*, October 2022. Santiago, Chile.
12. **H. Zhang, W. Tang, W. Na, P. Lee, J. Kim**, "Implementation of Generative Adversarial Network-CLS combined with Bidirectional Long Short-Term Memory for Lithium-ion Battery State Prediction," in April 2020, *Energy Storage by Elsevier Journals*
13. **F. Shaikh, N. Haworth, R. Wells, J. Bishop, S. K. Chatterjee, S. Banerjee, S. Laha**, "Compact Instrumentation for Accurate Detection and Measurement of Glucose Concentration Using Photoacoustic Spectroscopy," *IEEE Access* 2022, 10, 31885–31895.
14. **M. T. Islam, M. R. Jani, S. Rahman, K. M. Shorowordi, S. Nishat, D. Hodges, S. Banerjee, H. Efstathiadis, J. Carbonara, S. Ahmed**, "Investigation of Non-Pb All-Perovskite 4-T Mechanically Stacked and 2-T Monolithic Tandem Solar Devices Utilizing SCAPS Simulation," *SN Applied Sciences* 2021, 3, 1–12.
15. **D. Basavaraj, S. Tayeb**, "Towards a Lightweight Intrusion Detection Framework for In-Vehicle Networks," *Journal of Sensors and Actuator Networks* 2022, 11, 6. doi: 10.3390/jsan11010006
16. **M. Kareem and S. Tayeb**, (2022) "Securing Routing in Low Power and Lossy Networks," *Lecture Notes in Networks and Systems*, vol 358. Springer, Cham. doi: 10.1007/978-3-030-89906-6_23
17. **R. Skaggs-Schellenberg, D. Wright, S. Tayeb**, (2021). "A Secure Mixed Reality Framework for the Internet of Things," in Arai, K. (eds), *Lecture Notes in Networks and Systems*, vol 360. Springer, Cham. doi: 10.1007/978-3-030-89912-7_30
18. **D. Jacuinde-Alvarez, J. Dols, and S. Tayeb**, (2021, September). "A Real-Time Intelligent Intra-Vehicular Temperature Control Framework," *Lecture Notes in Networks and Systems*, vol 294. Springer, Cham. doi: 10.1007/978-3-030-82193-7_39 [Best Presentation]
19. **A. Bonasu, A. Stillmaker, and S. Tayeb**, "Low-Power Vehicular CAN Bus ASIC Implementation," *2022 13th Latin American Symposium on Circuits and Systems*, virtual (in-press, presented in March 2022)



Ag-tech Intelligent Systems Research Team and their Autonomous Robot



Pictured from left to right are:

Sydney Rivera (Electrical Engineering), **Vanessa Jauregui-Salgado** (Agricultural Business), **Ankit Sharma** (Computer Engineering), **Dr. Hovannes Kulhandjian**, **Nicholas Amely** (Electrical Engineering)

